REMARKS

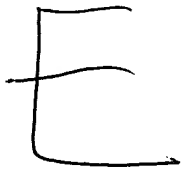
By this amendment, claim 28 has been canceled, and independent claims 10 and 11 have been amended to substantially incorporate the feature specified in claim 28. Claims 10, 11, and 18-27 remain in the application.

Claims 19, 22, and 25 were indicated to be drawn to allowable subject matter.

Claims 10, 11, 18, 20, 21, 23, 24, and 26-28 were rejected under 35 U.S.C. 102(e) as being anticipated by or, in the alternative, under 35 U.S.C. 103 as being obvious over U.S. Patent 5,434,452 to Higgins, III. The

Claims 18 and 24 each require that the interconnection layer include an "aluminum layer" and a "plating" on the aluminum layer. The "plating" contacts the bump electrodes, while the "aluminum layer" contacts the chip electrodes. This is best seen in the application at Figure 3d where the plating 62 overlies the aluminum layer 60. Contrary to the Examiner's assertion, the aluminum and plating are quite distinguishable from the drawing figures and serve to distinguish Higgins (which shows no plating of any sort). As explained on page 16 of the application, the plating serves the important functions of absorbing thermal stress and improving joint reliability with the bump electrode. At best, Higgins shows non-plated aluminum inside the wiring layer. Since Higgins lacks the plating, and necessarily lacks the required configuration of a plating contacting the bump and an aluminum layer contacting the chip electrode, the claimed invention set forth in claims 18 and 24, as well as the claims which depend therefrom, is not anticipated by or obvious over Higgins.

Claims 10 and 11 have been amended to require that



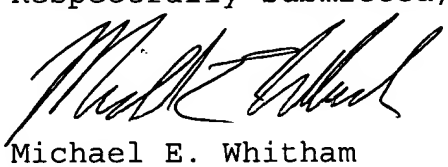
the interconnection layers extend from the periphery to the center. In the present invention, a semiconductor wafer (10) expands an alignment pitch of bump electrodes (70) by aligning the bump electrodes for connection of the semiconductor substrate that correspond to chip electrodes (11) formed along the periphery of each chip section (10a) in an entire surface including the center of the chip section.

Higgins, III discloses a mechanical integrated circuit (IC) wherein beam elements (20) are put between contact bumps (16) connected to a semiconductor chip and contact bumps (18) connected to a semiconductor substrate. The connections are made in a manner which maintains flexibility in the z-axis in a TAB (tape automated bonding) tape and the beam elements (20) act as cantileavered springs (see particularly column 4, lines 16-19). In addition, all of the beam elements (20) extend in one direction outside of the periphery as is best shown in Figures 12 and 13 of Higgins, III. Note particularly that the beam elements 20 in the most upper row extend outside an area of the semiconductor chip. Furthermore, the contact bumps 16 at the side of the semiconductor chip are primarily arranged in a central portion of the chip.

Accordingly, Higgins, III describes a mechanical IC which has structure that is different from that of the claimed invention. That is, the mechanical IC according to Higgins, III is used to attach a semiconductor device to a semiconductor substrate. In contrast, the claimed invention describes a semiconductor wafer which is dividable into chips where interconnection layers which extend between bump electrodes and chip electrodes in each chip section extend from the periphery toward the center of each chip section.

In view of the above amendments and arguments the claims should now be in condition for allowance. Reconsideration and allowance at an early date is requested.

Respectfully submitted,



Michael E. Whitham
Reg. No. 32,635

Whitham, Curtis & Whitham
Reston International Center
11800 Sunrise Valley Drive, Suite 900
Reston, VA 20191
703-391-2510